REMARKS

Upon entry of the foregoing amendment, Claims 1 and 3-23 are pending in this application. The Examiner rejected Claims 1, 2, 11, 12 and 20 under 35 U.S.C. 102(b) and rejected Claims 21-23 under 35 U.S.C. 103(a). The Examiner objected to Claims 3-10 and 13-19 but indicated that those claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 1 has been amended to include the recitation of Claim 2 and Claim 2 has been cancelled in the foregoing amendment.

Claims 1, 11, 12 and 20 Are Not Anticipated by *Zukowski*

The Examiner rejected Claims 1, 2, 11, 12 and 20 as anticipated by U.S. Patent No. 4,926,423 to Zukowski et al. ("*Zukowski*"). The Applicants traverse this rejection for the reasons discussed below.

Claim 1

Amended Claim 1 requires that the precoding circuit carries out the precoding such that the time division multiplexed output signal outputted by the time division multiplexer is equivalent to a signal that can be obtained by precoding a binary data signal having a bit rate equal to R that is time division multiplexed in units of one bit in advance.

In contrast, *Zukowski* only states regarding precoding that "the input signals D0 through D3 must first be "precoded" in such a way that when later combined by the merging network 23, the output of the network 25 will be the conventional time-division multiplexed form of the incoming data D0 through D3" (Column 8, lines 60-66), and the precoder as shown in Figs. 4A and 4B of *Zukowski* are substantially different from the precoding circuit of the present invention as shown, for example, in Fig. 6 or Fig. 13.

Thus, *Zukowski* in fact fails to disclose the precoding circuit that carries out the precoding such that the time division multiplexed output signal outputted by the time division multiplexer is equivalent to a signal that can be obtained by precoding a binary data

signal having a bit rate equal to R that is time division multiplexed in units of one bit in advance.

Accordingly, Claim 1 is not anticipated by *Zukowski*.

Claim 11

Dependent Claim 11 further requires a time division demultiplexer which time division demultiplexes binary data signals into n sets of the parallel input binary data signals which are to be entered into the precoding circuit, which is shown for example in Fig. 22.

In contrast, *Zukowski* discloses a time division demultiplexer 37 which time division demultiplexes the output of the multiplexer 36 as shown in Fig. 7. Therefore, *Zukowski* fails to disclose a time division demultiplexer for time division demultiplexing binary data signals having a bit rate equal to R, into the n sets of the parallel input binary data signals having a bit rate equal to R/n which are entered into the precoding circuit.

Accordingly, Claim 11 is also not anticipated by *Zukowski*.

Claim 12 and 20

Claims 12 and 20 have the limitations similar to that of Claims 1 and 11. The remarks made above in support of Claims 1 and 11 are also applicable to distinguish the dependent claims from *Zukowski*. Therefore, Claims 12 and 20 are not anticipated by *Zukowski*.

***Cominetti* Does Not Show or Suggest Claims 21-23**

The Examiner rejected Claims 21-23 as unpatentable over U.S. Patent No. 4,887,269 to Cominetti et al. ("*Cominetti* "). The Applicants traverse this rejection for the reasons discussed below.

The Examiner admitted in rejecting Claims 21-23 that *Cominetti* fails to disclose the specific arrangement of EXOR circuit, and D-type flip-flop or delay units as claimed. However, the Examiner then contended that it is well known in the art to form a differential

encoder that uses EXOR circuit, and D-type flip-flop or delay units in any desired configuration to fulfill the system specification and requirement.

However, *Cominetti* only discloses a conventional differential encoder configuration formed by the EXOR gate 52 and the delay circuit 54, which is similar to that shown in Fig. 3 (Prior Art) of the present specification. *Cominetti* completely fails to show or suggest the specific configuration of the differential encoder as recited in Claims 21-23, and shown in Fig. 15 (Claim 21) and Fig. 17 (Claims 22-23).

In particular, the configuration of Fig. 15 is specifically designed to shorten internal delay time as described on page 22, lines 2-5 of the specification. However, *Cominetti* does not show or suggest any teachings for shortening the internal delay time in the differential encoder.

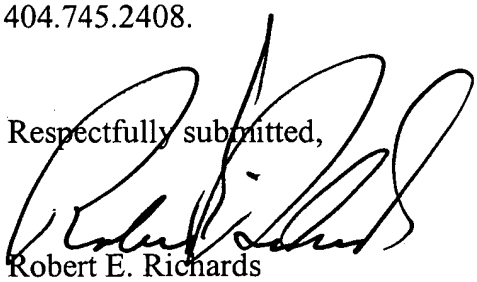
Likewise, the configuration of Fig. 17 is specifically designed to handle higher transmission rates as described on page 25, lines 2-14 of the specification. However, *Cominetti* fails to disclose any teachings for handling higher transmission rate.

Accordingly, Claims 21-23 would not have been obvious to one of ordinary skill from *Cominetti* at the time the Applicants made the claimed invention.

CONCLUSION

The foregoing is submitted as a complete response to the Office Action identified above. This application should now be in condition for allowance, and the Applicant solicits a notice to that effect. If there are any issues that can be addressed by telephone, the Examiner is asked to contact the undersigned at 404.745.2408.

Respectfully submitted,



Robert E. Richards
Reg. No. 29,105

KILPATRICK STOCKTON LLP
Suite 2800, 1100 Peachtree Street
Atlanta, Georgia 30309-4530
Our Docket: 44471-234029